Frame synchronizing device and method

The present invention relates to a frame synchronizing device for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, comprising a serial input parallel output shift register means for receiving said serial bit stream and outputting said frames in a

5   consecutive order, said shift register means including a serial input portion and a parallel output portion and having at least as many stages as the number of bits of a frame. Further, the present invention relates to a frame synchronizing method for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, comprising the steps of inputting said serial bit

10   stream into a serial input portion of a serial input parallel output shift register means having at least as many stages as the number of bits of a frame, and outputting said frames in a consecutive order from a parallel output portion of said shift register means.

Such a device and such a method is used in a digital data transmission systems like SDH (Synchronous Digital Hierarchy)/SONET (Synchronous Optical Network) or

15   Gigabit Ethernet and in particular in the networking part of such a system, where serial data are transported over a single channel and, at the receiving side, converted into parallel data for further processing.

In digital data transmission systems like SDH/SONET or Gigabit Ethernet, data at the transmitting side is sent byte after byte, forming an endless stream of bits in serial

20   order, wherein a byte is a word of ones and zeroes of fixed, but unimportant, length. When this sequence of bits has to be byte demultiplexed at the receiving side, it is crucial to know the position of the original bytes in this stream of bits. A transmission overhead gives the possibility to do so, by inserting one ore more special byte(s) at the transmit side, also known as frameheader bytes (SDH/SONET) or comma byte (Gigabit Ethernet). However, the time

25   moments of occurrence of this special byte is unknown at the receiving side so that special measures are required to recognize this special byte at the receiving side. When this special byte is recognized in the stream of bits at the receiving side, the moment of demultiplexing is known and the demultiplexed parallel output data can be aligned to the byte boundaries.

To be able to recognize the special byte at the receiving side, frameheader detection or comma byte detection is necessary and a resetable clock-divide-by-N counter must be synchronized to the frameheader byte position. This clock-divided-by-N output signal determines the moment when the demultiplexing occurs. The synchronization of this synchronous resetable clock-divide-by-N counter, when the special byte is detected, must be done at full operation speed in an exactly known time interval.

US 4,675,886 discloses a frame synchronization device which utilizes a frame alignment word decoder connected to the outputs of a shift register which receives at its input the received data bit stream. It is clocked by a clock signal generated from a selection of periods of the data bit stream timing signal reproducing a periodic pattern. This pattern is formed by relative bit locations within the duration of a frame certain at least of which are distributed according to the distribution of the bits of an alignment word in a frame and which form groups of the same size regularly distributed over the duration of a frame. This clock signal is generated in the device by a divider which divides by 20 or by 21 which imposes on it a periodic phase skip by the value of one period of the data bit stream timing for as long as the alignment word is not recognized by the decoder. The shift register is implemented in two parallel parts clocked by versions of the clock signal with a relative phase shift between them, one of which parts updates the other part in parallel on each phase skip of the clock signal.

US 5,442,636 describes a frame aligner circuit for aligning a plurality of information packet signals received within a maximum starting time variation interval, which circuit consists of a plurality of frame detectors, stretch circuits and variable delay circuits which are controlled by a synchronization signal generator and a delay control circuit. The delay control circuit in one embodiment of the present invention delays each information packet signal for a duration of time defined by the start of the information packet signal and an interval of time following the start of a last received information packet signals. In this manner, each information packet signal is delayed by a corresponding period of time to align the plurality of information packet signals with respect to one another.

WO 00/77960 discloses a method and a device for converting virtually concatenated data streams into contiguously concatenated data streams. The data are transmitted in containers, and N containers are combined in one multiframe. The virtually concatenated data streams consist of X partial streams/channels. Every container that is

allocated to the same location in the multiframe is identified by evaluating a multiframe

indicator of the container. The time-shift of said identified containers of the partial data

streams with respect to one another is measured. If such a time-shift is detected, only the

leading containers are delayed in such a manner that a time-wise alignment of all containers

5   is achieved. Every channel is correlated with a pointer interpreter, followed by an flexible

memory and a pointer generator. The pointer generators are inter-synchronized, and every

pointer generator is equipped to control the read-out of the flexible memory that pertains to

its channel. A channel selected as the master channel is provided with an overhead inserter.

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          It is an object of the present invention to improve the efficiency of the frame

synchronization and in particular to achieve a low power dissipation.

          In order to achieve the above and further objects, according to a first aspect of

the present invention, there is provided a frame synchronizing device for a binary data

15   transmission system wherein digital data are transmitted as a serial bit stream organized into

frames, each frame including a pre-defined frameheader, comprising a serial input parallel

output shift register means for receiving said serial bit stream and outputting said frames in a

consecutive order, said shift register means including a serial input portion and a parallel

output portion and having at least as many stages as the number of bits of a frame,

20   characterized by controlling means for detecting whether or not a frameheader is present at

the output of said parallel output portion and, if not, controlling said shift register means so

that the outputting of a frame from said parallel output portion is delayed by at least one time

period which is needed for shifting a bit in said serial input portion from a stage to a next one,

until synchronization is reached.

25   According to a second aspect of the present invention, there is provided a

frame synchronizing method for a binary data transmission system wherein digital data are

transmitted as a serial bit stream organized into frames, each frame including a pre-defined

frameheader, comprising the steps of inputting said serial bit stream into a serial input portion

of a serial input parallel output shift register means having at least as many stages as the

30   number of bits of a frame, and outputting said frames in a consecutive order from a parallel

output portion of said shift register means, characterized by the further steps of detecting

whether or not a frameheader is present in the output of said parallel output portion, and, if

not, delaying the outputting of a frame from said parallel output portion by at least one time

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period which is needed for shifting a bit in said serial input portion from a stage to a next one, until synchronization is reached.

According to the present invention, the outputting of a frame from the parallel output portion of the shift register is held for at least one high frequency cycle, and the moment of demultiplexing of the bit stream is skipped or "kicked" at least one bit. Namely, the demultiplexed parallel data outputted from the parallel output portion of the shift register means is fed to the controlling means which searches for the frame header. If the frame header is not found within a certain time, the demultiplexing is skipped at least one clock-cycle and consequently continued at least one bit later. This procedure is repeated until the frame header is detected in the parallel data. If it is detected, the system is synchronized. When the system has reached synchronization, meaning that the demultiplexed parallel output data is aligned to the byte boundaries, nothing happens anymore. Only when synchronization is lost again (e.g. due to external circumstances), the re-synchronization procedure will start over again.

A main advantage of the present invention is that the synchronization is done in the parallel clock domain having lower frequency and less dissipating or even by external sources like overall transmission system controllers. So, the synchronization according to the present invention can be implemented in a circuitry using low frequency driving signals, like CMOS.

It is noted that the term "frame" used herein means every kind of frame, word, byte etc. and that the term "frameheader" used herein means kind of special byte like e.g. frameheader byte (SDH/SONET) or, byte (Gigabit Ethernet).

Further advantageous embodiments of the present invention are defined in the dependent claims.

In particular, the delaying of the outputting of a frame may be repeated several times until synchronization is reached.

Usually, the frames have a fixed length, and, preferably, consist of bytes.

In a further embodiment wherein first clock pulses are generated which clock the outputting of the frames from the parallel output portion of the shift register means, the first clock pulses are delayed by at least one time period which is needed for shifting a bit in the serial input portion from a stage to a next one. So, the first clock pulses which may also be called output clock pulses are skipped by at least one clock pulse until synchronization is reached.

Usually, second clock pulses for clocking the inputting of the serial bit stream into the serial input portion of the shift register means are generated and converted into said first clock pulses having a time period which is N times longer than the time period of the second clock pulses, wherein each frame includes N bits, so that the first clock pulses are

5   delayed by at least one time period of said second clock pulses.

In a still further embodiment of the present invention, a ("kick-pin") control signal is generated, if a frameheader is not detected in the output of the parallel output portion of the shift register means, wherein the generation of the first clock pulses is blocked by said control signal for at least one time period which is needed for shifting a bit in the

10   serial input portion of the shift register means from a stage to a next one. So, such "kick-pin" signal determines skipping the first clock pulse until synchronization is reached.

The above described objects and other aspects of the present invention will be

15   better understood by the following description and the accompanying figures, in which:

Fig. 1 schematically shows the waveforms of the data bit signals at the transmitting side and at the receiving side;

Fig. 2 schematically shows the waveforms of the data bit signals at the transmitting side and at the receiving side including a frame header byte drawn as a shaded

20   portion;

Fig. 3 shows a schematic block diagram of a conventional frame synchronizing device comprising a serial input parallel output shift register;

Fig. 4 shows a schematic block diagram of a frame synchronizing device comprising a serial input parallel output shift register according to a preferred embodiment of

25   the present invention;

Fig. 5 a first preferred embodiment of a digital one shot circuit to be provided in the device of Fig. 4;

Fig. 6 shows waveforms of several signals used or created in the circuit of Fig. 5;

30   Fig. 7 shows waveforms of several signals used or created in the circuit of Fig. 5 when the Set signal occurs late with relation to the Clock-in-signal;

Fig. 8 shows a second preferred embodiment of a digital one shot circuit to be provided in the device of Fig. 4; and

Fig. 9 shows waveforms of several signals to be used or created in the circuit of Fig. 8.

5   In digital data transmission systems like SDH/SONET or Gigabit Ethernet, data at the transmit side (Tx) is sent byte after byte, forming an endless stream of bits in serial order as shown in Fig. 1. A byte being a word of ones and zeroes of fixed, but unimportant, length. When this sequence of bits has to be byte demultiplexed at the receive side (Rx), it is crucial to know the position of the original bytes in this stream of bits. The transmission

10   overhead gives the possibility to do so, by inserting one or more special byte(s) at the transmitting side, also known as frameheader bytes (SDH/SONET) or comma byte (Gigabit Ethernet), at for the receiving side unknown time moments. When this special byte is recognized in the stream of bits at the receiving side as indicated in Fig. 2, the moment of demultiplexing is known and the demultiplexed parallel output data can be aligned to the byte

15   boundaries.

To be able to recognize the special byte, frameheader detection or comma byte detection is necessary and a resetable clock-divided-by-N counter must be synchronized to the frameheader byte position. A conventional frame synchronizing device including such a resetable clock-divided-by-N counter is shown in Fig. 3. This clock-divided-by-N output

20   signal determines the moment when the demultiplexing occurs. The synchronization of this synchronous resetable clock-divided-by-N counter, when the special byte is detected, must be done at full operation speed in an exactly known time interval.

Present application proposes to use a so-called "kick-pin" principle which gives the possibility to synchronize the counter to the serial bitstream using low frequency

25   driving signals, like CMOS. Frameheader detection can then be done at the parallel data bit rate. The counter is not reset at an exactly known time moment, but the output clock is held for one high frequency clock cycle. The result of this action is that the moment of demultiplexing of the stream of bits is shifted one bit. This can be repeated at a low frequency until synchronization/alignment has taken place. Although the driving can be

30   operated at very low frequencies, it must be realized that synchronization will take much longer.

The demultiplexed data output is fed to a data handling device (a so-called framer circuit) which searches for the frameheader or comma byte in its inputted parallel data. If the special byte is not found within a certain time frame, it will send a signal to a

kick-pin of the clock-divided-by-N counter so as to skip one clock-cycle and consequently demultiplex one bit later. This procedure will repeat until the frameheader or comma byte is detected in the output parallel data. If it is detected, the system is synchronized. When the system has reached synchronization, meaning that the demultiplexed output data are aligned

5   to the byte boundaries, nothing happens anymore and the "kick-pin" signal will not be generated anymore. Only when synchronization is lost (e.g. due to external circumstances), the re-synchronization procedure will start over again.

The "kick-pin" signal in the device of Fig. 4 has the same role as the "Reset" signal in the device of Fig. 3, namely to adjust the time moment of demultiplexing. However,

10   the "Reset" signal in the device of Fig. 3 occurs in the high-frequency serial time domain, whereas the "kick-pin" signal in the device of Fig. 4 is created in the lower-frequency parallel time domain. Moreover, the "Reset" signal in the device of Fig. 3 sets the demultiplexing time moment instantaneously, whereas the "kick-pin" signal shifts the demultiplexing moment one clock cycle related to the serial high-frequency clock.

15   So, a main advantage is that the "kick-pin" signal can be generated by circuitry in the lower frequency, less dissipating parallel clock domain or even by external sources like overall transmission system controllers.

By the way, it should be mentioned that the serial clock is expected to be already extracted and correctly aligned to the serial data.

20   The circuit to skip one clock cycle can be provided as a so-called digital one shot. A first preferred embodiment of such a circuit is shown in Fig. 5. The circuit can be driven by a low frequency signal, while the output skips just one high frequency clock cycle.

When the "kick-pin" signal becomes high, the Q-output of a first flip-flop FF1 will become high at the next edge of clock-in. This sets the well-known set-reset circuit

25   (drawn here with or-gates) and kick-out will become high. The set signal is also fed to a second flip-flop FF2. The Q-output of this FF2 will then become high one clock cycle of clock-in later and consequently resets the set-reset circuit. Kick-out will go low again. Because S and R are never changing at the same time, forbidden states are impossible to occur. "AND"-ing the Kick-out signal with Clock-in gives a Clock-out signal which misses

30   one pulse. Applying this "missing-pulse-clock-signal" to a divide-by-N counter results in a "wait" time of one clock cycle. However, it should be noted that, because the set-reset circuit has unknown start-up behavior, the first kick-pin pulse might be necessary to get the circuit in a known state. The waveforms of the signals in the circuit of Fig. 5 are shown in Fig. 6.

When using N memory elements for FF2, the digital one shot can be extended to a so-called N-shot. For N=1, the set-reset circuit is not necessary and can be replace by a single gate. This is due to a correct timing-by-construction of two flip-flops in series.

Special care must be taken to avoid clock glitches. Namely, if the Set signal occurs late with relation to the Clock-in signal, the Clock-out signal will produce a pulse, exactly where it was intended not to have a pulse. Such a situation is shown in Fig. 7.

The actual circuit for removing one clock pulse from a continuous clock sequence as applied in Pathfinder chips is given in Fig. 8 showing a second preferred embodiment of a digital one-shot circuit. The maximum operating frequency of this circuit is determined by the delay of the inverter and the AND gate and by the set-up/hold time of the flip-flops. A third flip-flop FF3 should change first, then the second flip-flop FF2 and then the first flip-flop FF1. The waveforms of the signals used or occurred in the circuit of Fig. 8 are shown in Fig. 9.

Although the invention is described above with reference to examples shown in the attached drawings, it is apparent that the invention is not restricted to it, but can vary in many ways within the scope disclosed in the attached claims.